AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (ORIGINAL) An apparatus comprising:

a circuit configured to (i) change a frequency of one or more first signals in response to a second signal and (ii) generate a third signal in response to either said second signal or a predetermined time period expiring.

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2. (ORIGINAL) The apparatus according to claim 1, wherein said second signal programs said frequency.

3. (ORIGINAL) The apparatus according to claim 1, wherein said one or more first signals are generated by one or more phase lock loop circuits.

4. (ORIGINAL) The apparatus according to claim 3, wherein said second signal programs said one or more phase lock loop circuits.

5. (ORIGINAL) The apparatus according to claim 1, wherein said one or more first signals are generated using a divider network.

6. (ORIGINAL) The apparatus according to claim 1, wherein said predetermined time period is programmable.

7. (ORIGINAL) The apparatus according to claim 1, wherein said predetermined time period is started in response to said second signal.

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8. (ORIGINAL) The apparatus according to claim 1, wherein said circuit comprises a watchdog timer circuit that measures said predetermined time period.

9. (ORIGINAL) The apparatus according to claim 1, wherein one of said first signals is presented to a clock input of a processor and said third signal is presented to a reset input of said processor.

10. (ORIGINAL) The apparatus according to claim 9, wherein said second signal is generated using a number of instructions executed by said processor.

11. (ORIGINAL) The apparatus according to claim 10, wherein said instructions are contained in a computer readable medium.

12. (ORIGINAL) The apparatus according to claim 10, wherein said instructions are part of a basic input output system (BIOS) routine.

13. (ORIGINAL) The apparatus according to claim 9, wherein said predetermined time period expires only when said processor hangs.

14. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said circuit is further configured to generate a fourth ~~third~~ signal ~~has a first duration when generated~~ in response to ~~said second signal and a second duration when generated in response to~~ the expiration of said predetermined time period.

15. (ORIGINAL) The apparatus according to claim 1, wherein said circuit comprises an inter-integrated circuit (I^2C) interface circuit.

16. (ORIGINAL) The apparatus according to claim 1, wherein said circuit is configured to skew said one or more first signals.

17. (ORIGINAL) The apparatus according to claim 16, wherein said skew is programmable.

18. (ORIGINAL) An apparatus comprising:

means for changing a frequency of one or more first signals in response to a second signal; and

means for generating a third signal in response to either said second signal or a predetermined time period expiring.

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19. (ORIGINAL) A method for recovering in a phase lock loop circuit from a processor hang due to over-clocking comprising the steps of:

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(A) changing a frequency of a clock signal;

(B) resetting said processor in response to said frequency change; and

(C) detecting whether said processor hangs in response to said frequency change.

20. (ORIGINAL) The method according to claim 19, further comprising the step of:

(D) when said processor hangs, changing said frequency of said clock signal to a fail-safe frequency and resetting said processor.

Please add the following new claim:

Sub B/ cncl
A7 cncl

21. (NEW) The apparatus according to claim 14, wherein: said third signal is configured to reset a processor; and said fourth signal is configured to reset an entire system.